(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 373 672 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 89123262.1

(22) Date of filing: 15.12.89

(51) Int. Cl.[5]: G11C 11/409

(30) Priority: 16.12.88 JP 317827/88

(43) Date of publication of application: 20.06.90 Bulletin 90/25

(84) Designated Contracting States: DE FR GB

(71) Applicant: NEC CORPORATION
33-1, Shiba 5-chome, Minato-ku
Tokyo 108(JP)

(72) Inventor: Fujii, Takeo
c/o NEC Corporation 33-1, Shiba 5-chome
Minato-ku Tokyo(JP)

(74) Representative: Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62 Liebherrstrasse 20
D-8000 München 26(DE)

DOC

(54) Semiconductor memory circuit having an improved restoring control circuit.

(57) A dynamic memory circuit which can operate with a reduced amount of current noise and without destruction of stored data is disclosed. The memory circuit includes dynamic memory cells necessitating restoring operation, a read circuit for performing a read-out operation in an active state and a restore circuit for performing a restore operation in a reset state following the active state.

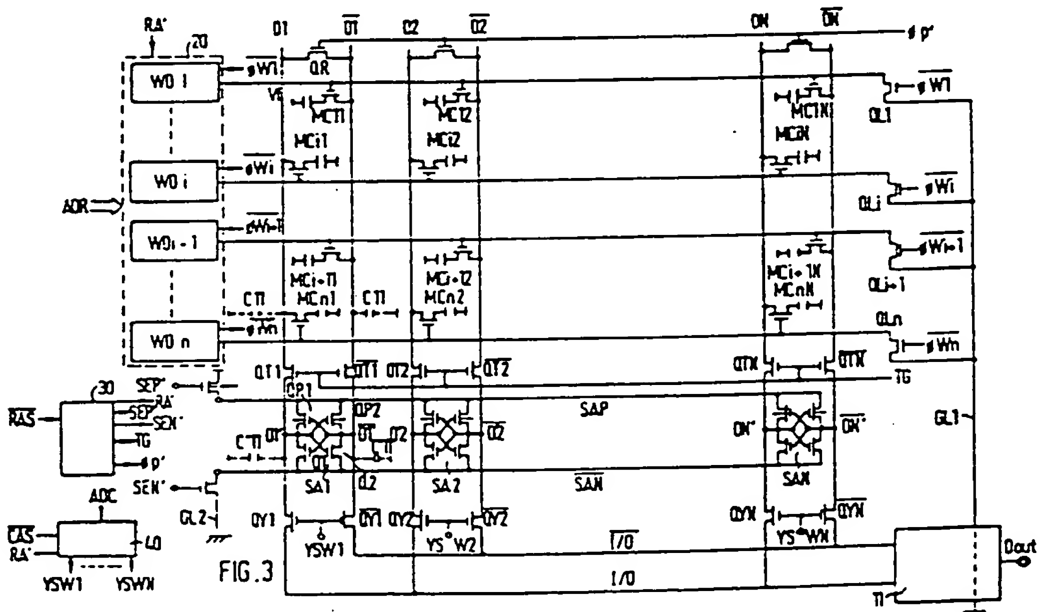


FIG.3

EP 0 373 672 A2

SEMICONDUCTOR MEMORY CIRCUIT HAVING AN IMPROVED RESTORING CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a semiconductor memory circuit and, more particularly to a dynamic type random access memory (DRAM) fabricated on a semiconductor substrate.

Description of the Related Art:

Dynamic memory circuits have been widely utilized as large capacity semiconductor memories in various fields. The dynamic memory circuit is generally constructed in such a manner that one-transistor type memory cells are arranged in a matrix form of rows and columns together with word lines and bit lines arranged in rows and columns, respectively.

According to the conventional technique, the number of memory cells connected to one bit line increases as the memory capacity increases. Consequently, a stray capacitance of each bit line increases to cause various problems. First, when the sense amplifiers are activated, the bit lines need to be charged or discharged to a power supply potential Vcc or a ground potential Vss. In this regard, the increase in the stray capacitances of the bit lines cause an increase in the time required for charging and discharging. If the respective pairs of bit lines are not sufficiently amplified, that is, if charging or discharging is not sufficiently effected, it is impossible to enable a column selection circuit so as to connect the selected pair of bit lines to a pair of common data lines. This is because, when the common data lines are connected to bit lines, the charges on the common data lines may flow into the bit lines to destroy the stored information. In consequence, the time at which the data is output from an output terminal is delayed, which results in a lower operation speed. Secondly, the increase in the bit line stray capacitances causes an increase in the charging and discharging current during an active period, thus causing problems, for example, floating of the ground potential at an internal ground wiring, a lowering in the power supply potential, and generation of noise between the bit lines. Particularly, the floating of the ground potential during the active period causes a noise due to operations of peripheral circuits such as an output circuit, the column selection circuit, and a potential of the non-selected word lines undesirably exceeds a threshold voltage of memory cell transistors or more, storage capacitors of the non-selected memory cells are erroneously connected to the bit lines, resulting in destruction of the stored data.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor memory circuit which can operate at a high speed.

It is another object of the present invention to provide a dynamic memory circuit which can stably operate without data destruction.

The dynamic memory according to the present invention comprises means for receiving an external control signal having a first level which sets the memory in an active state and a second level which sets the memory in a reset state and dynamic memory cells which require restoring read-out data therein and, is featured in that read-out of data from a memory cell or cells is performed in the active state and restoring of data to the memory cell or cells is conducted in the reset state.

According to a preferred aspect of the present invention, a time required for the restoring of data to the memory cells is removed in the active state can be shortened and a current amount required in the active state is reduced.

Moreover, bit lines are not charged or discharged in the active state but left near a precharged level with small signal difference, memory cell transistors of the memory cells coupled to the non-selected word lines are never turned conductive even when the potential of the non-selected word lines float in levels. Thus, destruction of data stored in the non-selected memory cells can be effectively prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further objects, features and advantages of the present invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a schematic circuit diagram showing a dynamic memory in the prior art;

Fig. 2 is a timing diagram showing an operation of the memory of Fig. 1;

Fig. 3 is a schematic circuit diagram of a dynamic memory according to a first embodiment of the present invention;

Fig. 4 is a timing diagram showing an opera-

tion of the memory of Fig. 3;

Fig. 5 is a schematic block diagram of a timing signal generator employed in the memory of Fig. 3;

Fig. 6 is a timing diagram showing waveforms of signals in the timing signal generator of Fig. 5;

Fig. 7 is a schematic circuit diagram of a dynamic memory according to a second embodiment of the present invention: and

Fig. 8 is a timing diagram showing an operation of the memory of Fig. 7.

DETAILED DESCRIPTION OF THE INVENTION

Description of the Prior Art:

With reference to Figs. 1 and 2, a typical structure of the conventional dynamic memory will be explained.

As shown in Fig. 1, the memory comprises a plurality of one-transistor type memory cells MC_{11} - MC_{nN} each having a memory cell transistor Q_M and a storage capacitor C_M connected between the transistor Q_M and a fixed potential V_f, word lines WL_1 - WL_n arranged in rows, a plurality of bit line pairs D_1, $\overline{D_1}$ - D_N, $\overline{D_N}$ arranged in columns, CMOS type sense amplifiers SA_1 - SA_N provided for the bit line pairs D_1, $\overline{D_1}$ - D_N, $\overline{D_N}$, respectively, a pair of common data lines I/O, $\overline{I/O}$, a plurality of pairs of column selection transistors QY_1, QY_1' - QY_N, QY_N' connected between the bit line pairs and the pair of common data lines, respectively, a row decoder 20 having decoding units WD_1 - WD_n for selecting the word lines WL_1 - WL_n, and an output circuit 11.

The row decoder 20 operatively selects one of the word lines WL_1 - WL_n in accordance with row address signals ADR in response to a timing signal RA. Each of the sense amplifiers SA_1 - SA_N includes P-channel MOS transistors QPl, QP2 and N-channel MOS transistors Q1, Q2 and is connected to a first activation line SAP and a second activation signal $\overline{SAN}$. The activation line SAP is connected to a p-channel MOS transistor QP_3 controlled by a control signal SEP and the activation line $\overline{SAN}$ is coupled to an N-channel MOS transistor Q_{10} controlled by a control signal SEN. The pairs of column selection transistors QY_1, QY_1' - QY_N, QY_N' are controlled by column decoder signals YSW_1 - YSW_N generated by a column decoder (not shown) in a known way.

The row decoder 20 also generates clamp signals $\overline{\phi_{w1}}$ - $\overline{\phi_{wn}}$ which are opposite to those outputs for the word lines WL_1 - WL_n, respectively. For example, when the word line WL_1 is selected (high level), the signals $\overline{\phi_{w2}}$ - $\overline{\phi_{wn}}$ are high in level with $\overline{\phi_{w1}}$ at a low level. Clamp transistors of N-channel type QL_1 - QL_n are connected between the word lines WL_1 - WL_n and a ground wiring GL_1 which is extending through the output circuit 11 and connected to the output circuit 11. The clamp transistors QL_1 - QL_n receive the clamp signals $\overline{\phi_{w1}}$ - $\overline{\phi_{wn}}$, respectively. While the source of the transistor Q_{10} is connected to a separate ground wiring GL_2.

With reference to Fig. 2, a typical operation of the memory of Fig. 1 will be explained.

During a reset period TP_1 before the starting (t_1) of the active operation period (T_A), the bit lines D_1, $\overline{D_1}$ to D_N, $\overline{D_N}$ have been maintained at, for example, an intermediate potential (1/2 Vcc) of a power supply potential Vcc and a ground potential Vss. When the row address strobe signal $\overline{RAS}$ becomes an active, low level at t_1, the active period T_A is initiated and one word line driving circuit, for example, WDi, is selected among the word line driving circuits WD_1 to WD_n on the basis of row address signals ADR given externally in response to RA which is an internal signal formed front $\overline{RAS}$ at t_2, so that one selected word line e.g. WLi rises in potential. In consequence, the memory cell transistors Q_M of the memory cells MCil to MCiN turn ON, so that the potentials of one bit lines of the bit line pairs D_1, $\overline{D_1}$ to D_N, $\overline{D_N}$ change in the range of from about 100 mV to 200 mV in accordance with charges stored in the respective storage capacitors C_M. On the other hand, the potentials of the other bit lines remain at the initial value, that is, the potential of 1/2 Vcc. Accordingly, the signals representative of the potential differences are input to the sense amplifiers SA_1 to SA_N, respectively. Next, when the sense amplifier enabling signal SEN rises and SEP falls at t_3, the sense amplifiers SA_1 to SA_N are activated to amplify the very small difference signals input to the sense amplifiers. As a result, for example, the bit line D_1 lowers to the ground potential, while the bit line $\overline{D_1}$ rises to the power supply potential Vcc (in the case where the memory cell MCil has "0" information (L) stored therein). In actual fact, the information in the capacitor C_M of the memory cell MCil is destroyed through the exchange of charges with the bit line D_1 when the word line WLi rises to read out information to the bit line D_1. Therefore, the above-described sense amplifier operation serves not only to amplify the very small signals on the bit lines D_1 and $\overline{D_1}$ but also to rewrite (i.e., refresh) the destroyed information to the memory cell by reading out the signals to the bit lines. Thereafter, the column decoder signal YSW, which is an internal signal generated from a column address strobe $\overline{CAS}$ on the basis of column address signals (not shown) given to an external address terminal in response to the fall of the column address strobe $\overline{CAS}$, rises, so that, for example, YSW_1 is selected

and rises at t_5. As a result, the data from the bit line pair D_1 and $\overline{D_1}$ is transferred to the common data line pair I/O and $\overline{I/O}$. The transferred data is amplified by the output circuit 11 and output to the outside from the output terminal Dout. Then, the active period T_A is terminated at t_6 and the reset signal ϕ_p rises at t_7.

In the above-described prior art, as the storage capacity increases, the number of memory cells connected to each bit line increases and consequently the stray capacitances C_{31} of the bit lines increase, thus causing various problems. First, when the sense amplifiers are activated as described above, the bit lines D_1 to D_N and $\overline{D_1}$ to $\overline{D_N}$ need to be charged or discharged to the power supply potential Vcc or the ground potential Vss; in this regard, the increase in the stray capacitances C_{31} of the bit lines cause an increase in the time required for charging and discharging. If the bit line pairs D_1, $\overline{D_1}$ to D_N, $\overline{D_N}$ are not sufficiently amplified, that is, if charging or discharging is not sufficiently effected, it is impossible to enable YSW so as to connect bit lines to the common data lines I/O and $\overline{I/O}$. This is because, when the common data lines are connected to bit lines, the charges on the common data lines may flow into the bit lines to destroy the information. In consequence, the time at which the data is output from the output terminal Dout is delayed, which results in the performance being deteriorated. Secondly, the increase in the bit line stray capacitances C_{31} invites an increase in the charging and discharging current, thus causing problems, for example, floating of the ground potential, a lowering in the power supply potential, and generation of noise between the bit lines.

Moreover, in the above-described conventional semiconductor memory, either the bit line D_1 or $\overline{D_1}$ is discharged to the ground potential during the active period T_A when the row address strobe signal $\overline{RAS}$ is at the low potential. Therefore, if a noise is generated in the internal grounding wiring GL_1 due to the activation of the output circuit 11 during this period, the potentials of the wiring GL_1 and the non-selected word lines, for example, WLi + 1, undesirably rises from the ground potential to a potential near the threshold voltage of the memory cell transistors Q_M, while the bit line D_1 already becomes the ground potential, and if the memory cell MCi + 11 has information "1" (H) stored therein, the sub-threshold current of the MOS transistor in the memory cell MCi + 11 causes the charge in the capacitor of the memory cell MCi + 11 to flow out to the bit line D_1, thus causing destruction of the stored information. Since this phenomenon is caused by the sub-threshold current of the MOS transistor in the memory cell, failures are likely to occur frequently due to variations in manufacture, for example, misalignment, variations in the gate length of the gate electrodes, etc. The worst is the case where the row address strobe signal $\overline{RAS}$ is maintained at the low potential for a long period of time and during this period the column address strobe signal $\overline{CAS}$ and the external address signal change at high frequency. Thus, a great deal of time is required for inspection.

Description of Preferred Embodiments:

With reference to Figs. 3 to 6, the dynamic memory according to one embodiment of the present invention will be explained. In Figs. 3 to 6, elements or portions corresponding to those in Figs. 1 and 2 are denoted by the same or similar references and detailed description therefor will be omitted.

The memory of this embodiment is featured as follows. Namely, a plurality of pairs of transfer gate (N-channel) transistors QT_1, $\overline{QT_1}$ - QT_N, $\overline{QT_N}$ are inserted between the pairs of bit lines D_1, $\overline{D_1}$ - D_N, $\overline{D_N}$ and a plurality of pairs of sense nodes D_1', $\overline{D_1}'$ - D_N', $\overline{D_N}'$ of the sense amplifiers SA_1 - SA_N, respectively. The purpose of provision of the transfer gates Q_{T1} to $\overline{Q_{TN}}$ is to cut off the bit line stray capacitances C_{11} from the stray capacitances C_{11}' of the sense nodes D_1' to $\overline{D_N}'$ when the sense amplifiers are activated, thereby increasing the operating speed of the sense amplifiers.

A timing signal generator 30 receives the row address strobe signal $\overline{RAS}$ and generates timing signals RA', SEP', SEN', TG and ϕ_p'. A column decoder 40 receives column address signals ADC and generates the column decoder signals YSW_1 - YSW_N under control of $\overline{CAS}$ and RA'.

In addition, a restoring or rewriting operation is conducted during a reset period when $\overline{RAS}$ is made inactive under control of RA', SEP', SEN', TG and ϕ_p' generated by the timing signal generator 30.

The operation of the memory of Fig. 3 will be explained with reference to Fig. 4.

Prior to a time point t_1, a reset period TP_1 has been set and the pairs of bit lines D_1, $\overline{D_1}$ - D_N, $\overline{D_N}$ and the sense nodes D_1', $\overline{D_1}'$ - D_N', $\overline{D_N}'$ have been precharged to a precharge potential (1/2 Vcc level). At t_1, the row address strobe signal $\overline{RAS}$ becomes active (low level) to introduce the active period the row address signals ADR are taken in, and on the basis of this address signals one word line driving unit, for example, WDi, is selected from among the word line driving circuits WD_1 to WD_n. Thereafter, as the internal signal RA' formed on the basis of $\overline{RAS}$ rises at t_2, the potential of the selected word line WLi rises and consequently information stored in the memory cells MCi_1 to MCi_N connected to thr selected word line WLi

appear as very small signals on the bit line pairs D_1, $\overline{D_1}$ to D_N, $\overline{D_N}$, respectively. Since at this time the transfer gate control signal TG is at the high potential, the signals on the bit line pairs D_1, $\overline{D_1}$ to D_N, $\overline{D_N}$ are also transferred to the sense nodes D_1', $\overline{D_1'}$ to D_N', $\overline{D_N'}$ respectively. Next, at t_3 the control signal TG is lowered to turn OFF the transfer gates Q_{T1} to $\overline{Q_{TN}}$, thereby cuttint off the bit lines D_1 to $\overline{D_N}$ from the sense nodes D_1' to $\overline{D_N'}$. Thereafter, at t_4 the sense amplifier enabling signals SEN' and SEP' are raised and lowered, respectively, to activate the sense amplifiers SA_1 to SA_N. Since the sense nodes D_1' to D_N' have relatively small stray capacitances C_{11}', as described above, they are amplified at high speed. As a result, for example, one sense node D_1' reaches the power supply potential Vcc, while the other sense node $\overline{D_1'}$ reaches the ground potential, rapidly. Thereafter, the column selection transistors, for example, Q_{Y1} and $\overline{Q_{Y1}}$, selected after the column address strobe signal $\overline{CAS}$ becomes active at t_5 on the basis of the externally applied column address information ADC, are driven to turn ON in response to the rise of the internal signal YSW at t_6 generated on the basis of $\overline{CAS}$, so that the data from the sense nodes D_1' to $\overline{D_1'}$ is transferred to the common data line pair I/O and $\overline{I/O}$ and output from the output terminal Dout via the output circuit 11. At this point of time, the transfer gate control signal TG remains at the low potential and therefore the bit lines D_1 to $\overline{D_N}$ are not charged nor discharged but maintained near the middle potential.

Therefore, it is guaranteed that the potentials of all the bit lines are near the 1/2 Vcc level and higher than the non-selected word lines even if the potential of the ground wiring GL_1 rises to some extent due to the operation of the output circuit 11. Ancordingly, the memory cell transistors Q_M of the memory cells coupled to the non-selected word lines are never turned ON.

Thereafter, when $\overline{RAS}$ and $\overline{CAS}$, become inactive at t_8 to introduce to a reset period TP_2, the internal signal YSW is first lowered to turn OFF the column selections transistors Q_{Y1} and $\overline{Q_{Y1}}$, thereby cutting off the sense nodes D_1' and $\overline{D_1'}$ from the common data line pair I/O and $\overline{I/O}$. Thereafter, at t_9 the transfer gate control signal TG is raised to start charging and discharging of the bit lines D_1 to $\overline{D_N}$ by the sense amplifiers SA_1 to SA_N which have been left activated. Thus, one of each bit line pair D_1, $\overline{D_1}$ to D_N, $\overline{D_N}$ reaches the power supply potential Vcc, while the other reaches the ground potential, performing a restore operation. Thereafter, the word line driving signal RA' is lowered to lower the selected word line WLi. At this point of time, the refreshing of the memory cells MCil to MCiN is completed. Thereafter, the sense amplifier enabling signals SEN' and SEP' are reset at t_{10} and the bit line sense nodes are also reset, thus completing the operation.

In the foregoing, the arrangement in which N-type MOS transistors are employed as switching elements and CMOS type sense amplifiers are used has been described. However, various changes and modifications may be made to matters of design, for example, the selection of the above-mentioned parts and the set values for the initial and finally reached potentials, of the bit lines according to circumstances. The subject matter of the present application resides in that after the information stored in a memory cell has been transferred to the sense nodes during the active period, the sense nodes and the bit lines are left cut off from each other so as not to carry out charging or discharging of the bit lines. According to the present embodiment, the restoring data to the memory cells is conducted during the reset period after the active period T_A, and therefore, the effective length of the active period is shortened as viewed from the outside of the memory, thus, data rate in the access operation can be improved.

Moreover, the memory cell transistors Q_M of the non-selected memory cells are kept non-conductive by performing the restore operation in the reset period, destruction of stored data can be effectively prevented.

An example of the timing signal generator 30 in Fig. 3 will be explained with reference to Figs. 5 and 6.

As shown in Fig. 5, the timing signal generator 30 includes delay circuits D1 to D7, inverting delay circuits ID1 and ID2, inverter circuits IV_1 to IV_{10}, a dummy row address buffer 51, NAND gates 52, 54, 55, 56 and 57, a NOR gate 53, and a series circuit of P-channel MOS transistor QP_5 and N-channel MOS transistors Q_{51}, Q_{52}.

An internal signal ϕ_1 is generated from $\overline{RAS}$ through the delay circuit D1 and the inverter IV_2 and has the substantially opposite phase to $\overline{RAS}$. A control signal AE which is used to enable row address buffers (not shown in Fig. 3) is generated from the delay circuit D3. The dummy row address buffer 51 receives one of row address signals Ai and generates its true and complementary buffered signals Xi, $\overline{Xi}$ when enabled by AE. The signals Xi, $\overline{Xi}$ are applied to the NOR gate 53, the inverter IV_3 and the delay circuit D4 in cascade and, an internal signal ϕ_2 is generated when the states of Xi and $\overline{Xi}$ are established. The internal signals ϕ_1 and ϕ_2 are applied to the NAND gate 54 for generation of RA' and TG, as illustrated.

Internal waveforms of the respective signals are shown in Fig. 6.

Fig. 7 shows the arrangement of a second embodiment of the present invention. This arrangement differs from the arrangement shown in Fig. 3

in that bit lines are divided into two groups d_{1a}, $\overline{d_{1a}}$-d_{Na}, $\overline{d_{Na}}$ and d_{1b}, $\overline{d_{1b}}$-d_{Nb}, $\overline{d_{Nb}}$, which are separated from each other through second transfer gates Q_{T1}', $\overline{Q_{T1}}'$ to Q_{TN}', $\overline{Q_{TN}}'$.

The operation is substantially the same as that of the foregoing first embodiment except for the following. Namely, at the time when the transfer gate control signal TG is lowered at t_3 in the first embodiment in the active period T_A, the first and second transfer gate control signals TG and TG2 of the second embodiment are lowered simultaneously or successively in the mentioned order and thereafter both maintained at the low potential during the active periot T_A to maintain the bit lines d_{1a}, $\overline{d_{1a}}$ to d_{Na}, $\overline{d_{Na}}$ and d_{1b}, $\overline{d_{1b}}$ to d_{Nb}, $\overline{d_{Nb}}$ near the middle potential. In the reset period TP2 introduced by the fall of $\overline{RAS}$ at t_a, the control signal TG is raised and the control signal TG2 is raised with a little delay at t_2. In other words, the feature of the second embodiment resides in that the bit lines are divided and charged or discharged in a time division manner at the time of refreshing. Thus, it is possible to reduce the generation of noise.

As has been described above, according to the present invention, after the information stored in a memory cell has been transferred to the sense nodes during the active period, the sense nodes and the bit lines are cut off from each other so as to maintain the bit line potential near the middle potential between the power supply potential and the ground potential, thereby making it possible to prevent destruction of the information stored in non-selected memory cells due to floating or sinking of the non-selected word lines caused by the ground potential line noise in the chip that is attendant on the operations of other circuit blocks on the same chip, for example, the $\overline{CAS}$ circuit block, column address buffer and column address decoder circuit, during the active period.

Further, since the margin with respect to the sub-threshold current of the MOS transistors of the memory cells increases, the allowance for variations in manufacture is made. It it therefore possible to expect an increase in the production yield and it also becomes possible to shorten the channel and lower the threshold voltage of the MOS transistors of the memory cells. Thus, it is possible to reduce the size of memory cells and hence the overall size of the chip and improve the performance as a result of achievement of high-speed operation.

Claims

1. A semiconductor memory circuit comprising a plurality of dynamic type memory cells which necessitate restoring of read-out data for continuing storage of data, means for receiving an external control signal having an active level and an inactive level, means for operatively reading data from a selected memory cell in response to the active level of said external control signal and means for operatively restoring the data read from said selected memory cell into said selected memory cell in response to the inactive level of said external control signal.

2. The memory circuit according to claim 1, further comprising a plurality of word lines coupled to said memory cells, means for selecting one of said word lines in response to the active level of said external control signal, a plurality of bit lines coupled to said memory cells, a plurality of sense amplifiers coupled to said bit lines, a first reference voltage wiring coupled to said sense amplifiers, and a second reference voltage wiring coupled to said selecting means and said reading means.

3. The memory circuit according to claim 1, in which each of said memory cells includes a storage capacitor and a transfer gate transistor.

4. The memory circuit according to claim 1, in which said reading means includes a common data line, and an output circuit coupled to said common data line.

5. The memory circuit according to claim 1, further comprising a plurality of bit lines coupled to said memory cells, each of said bit lines being divided into first and second segments, and a plurality of transfer gates inserted between the first and second segments of said bit lines.

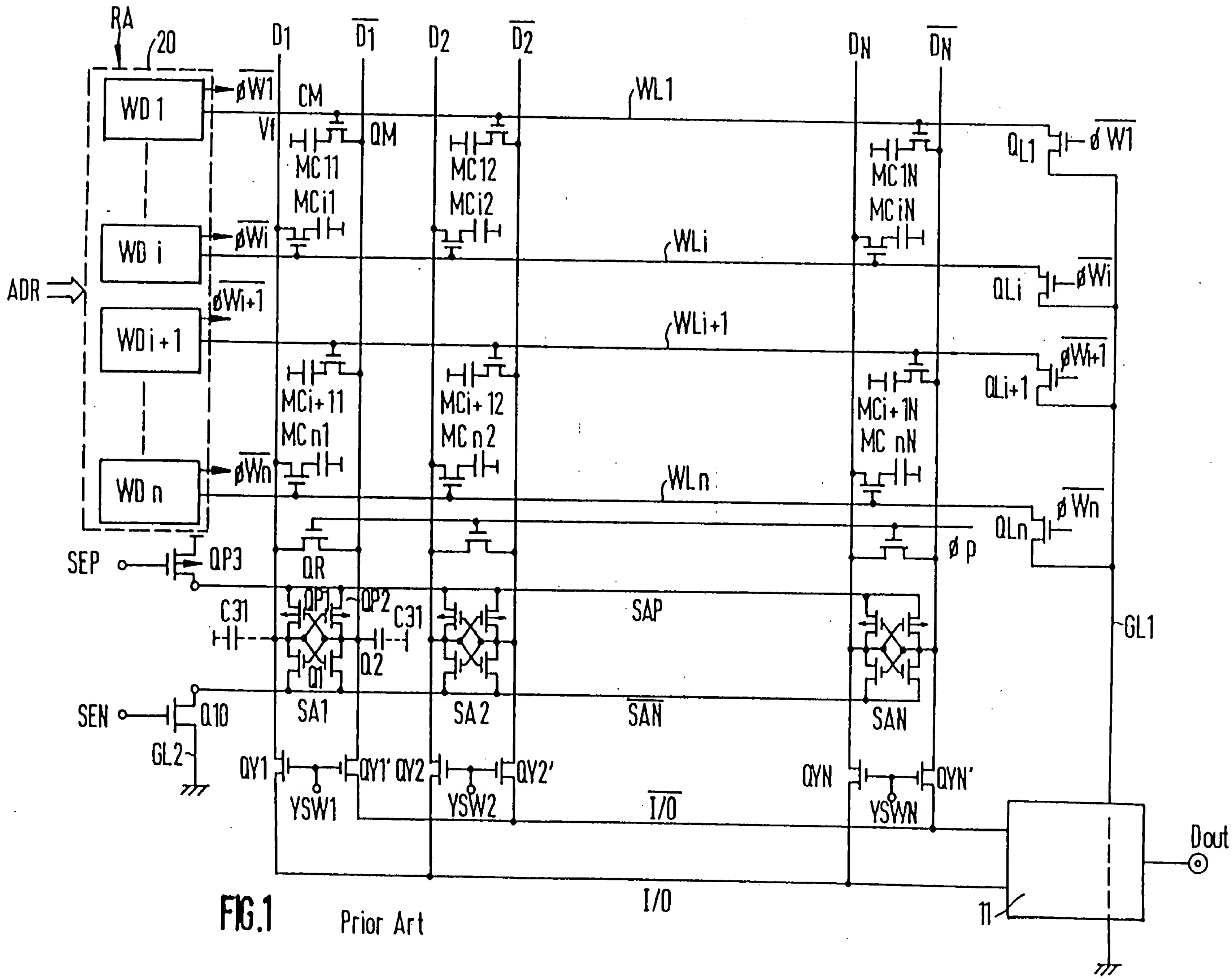


FIG.1 Prior Art

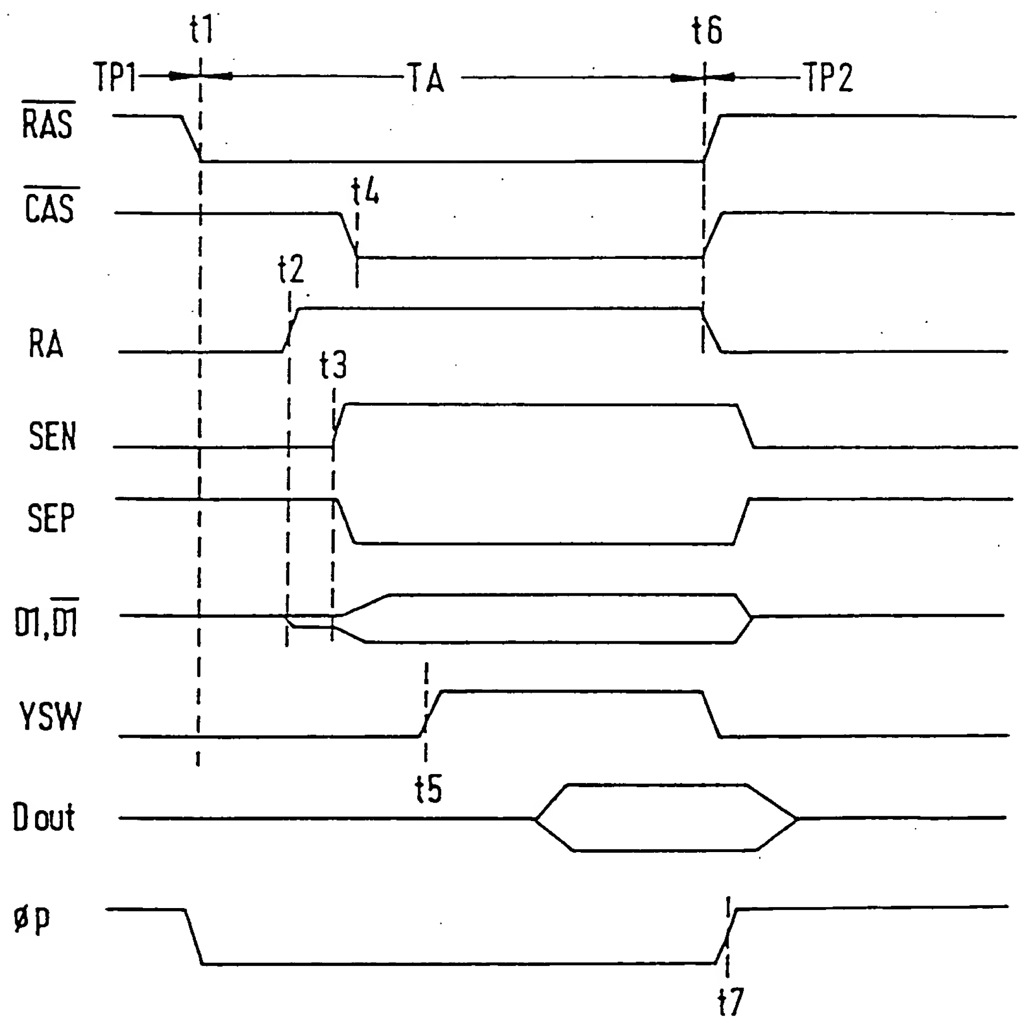


FIG.2 Prior Art

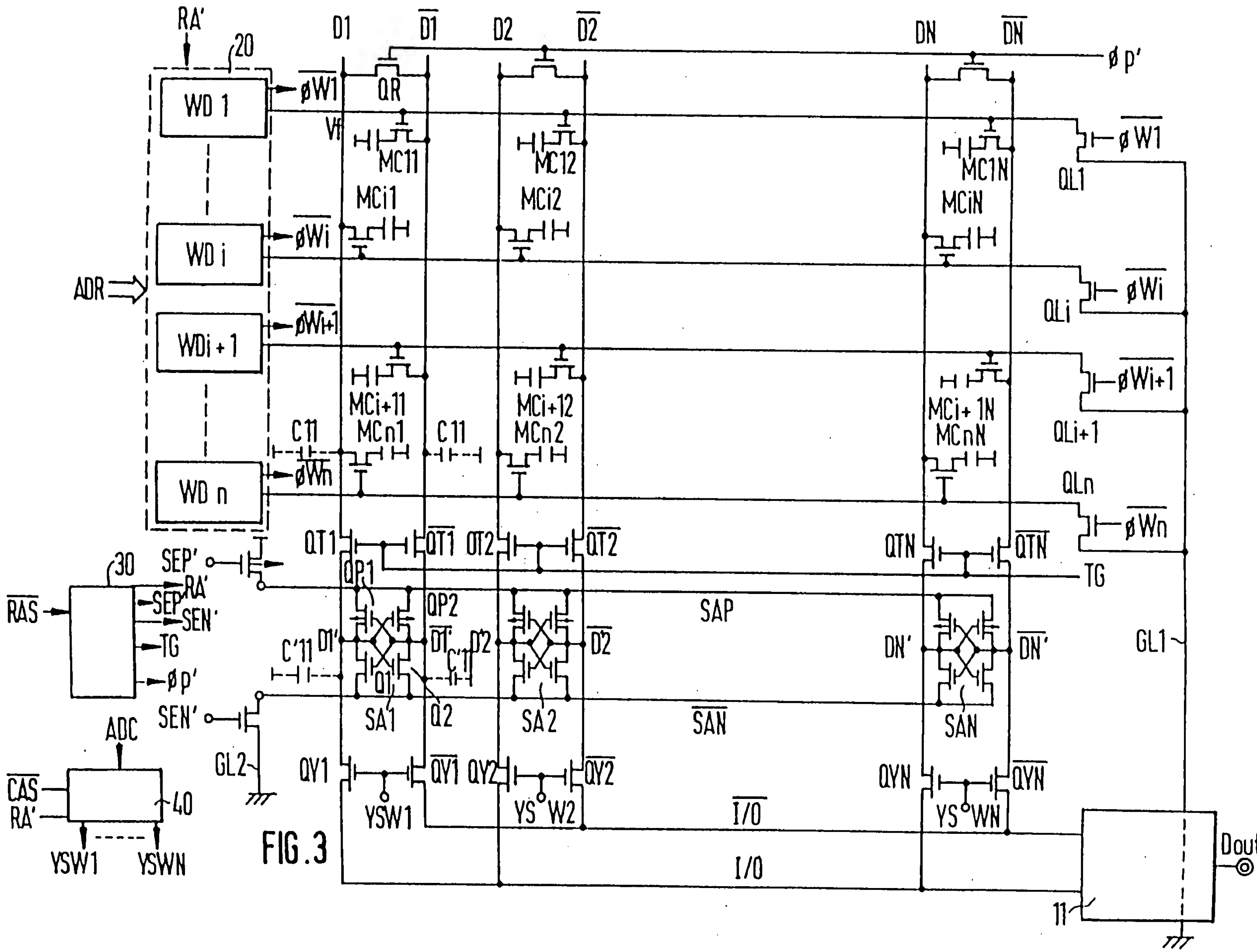

RA'
20
WD 1
WD i
WDi + 1
WD n
ADR
D1
$\overline{D1}$
D2
$\overline{D2}$
DN
$\overline{DN}$
ø p'
QR
Vf
MC11
MC12
MC1N
MCi1
MCi2
MCiN
MCi+11
MCi+12
MCi+ 1N
MCn1
MCn2
MCnN
C11
QL1
QLi
QLi+1
QLn
QT1
$\overline{QT1}$
QT2
$\overline{QT2}$
QTN
$\overline{QTN}$
TG
SEP'
30
$\overline{RAS}$
QP1
QP2
SAP
D1'
$\overline{D1'}$
D'2
$\overline{D'2}$
DN'
$\overline{DN'}$
C'11
Q1
Q2
SA1
SA2
SAN
$\overline{SAN}$
SEN'
GL1
GL2
ADC
$\overline{CAS}$
40
YSW1
YSWN
QY1
$\overline{QY1}$
QY2
$\overline{QY2}$
QYN
$\overline{QYN}$
YS W2
YS WN
$\overline{I/O}$
I/O
11
Dout

FIG. 3

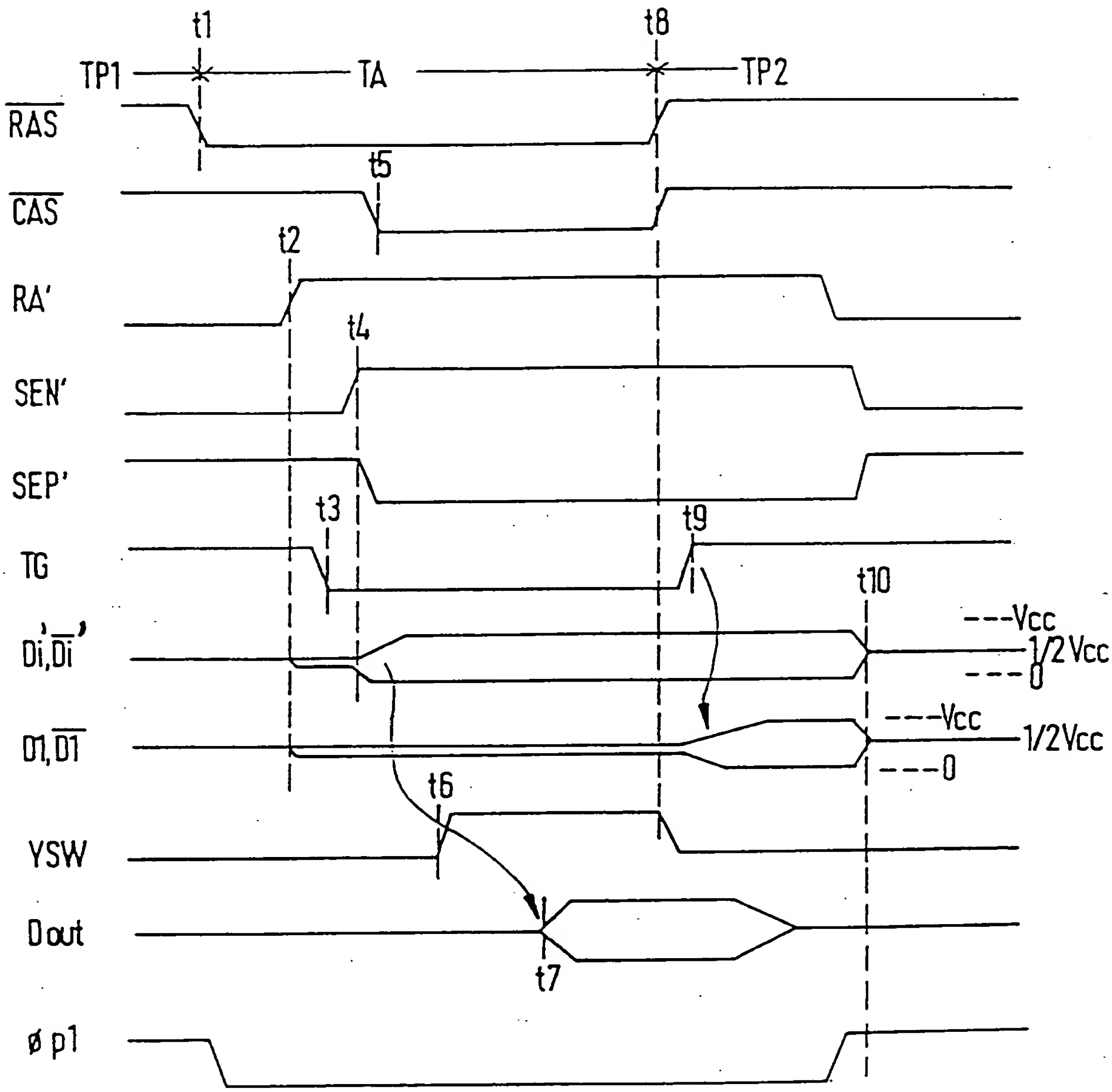

t1
t8
TP1
TA
TP2
RAS
t5
CAS
t2
RA'
t4
SEN'
SEP'
t3
t9
TG
t10
Vcc
Di',Di'
1/2Vcc
0
Vcc
D1,D1
1/2Vcc
0
t6
YSW
Dout
t7
ø p1

FIG.4

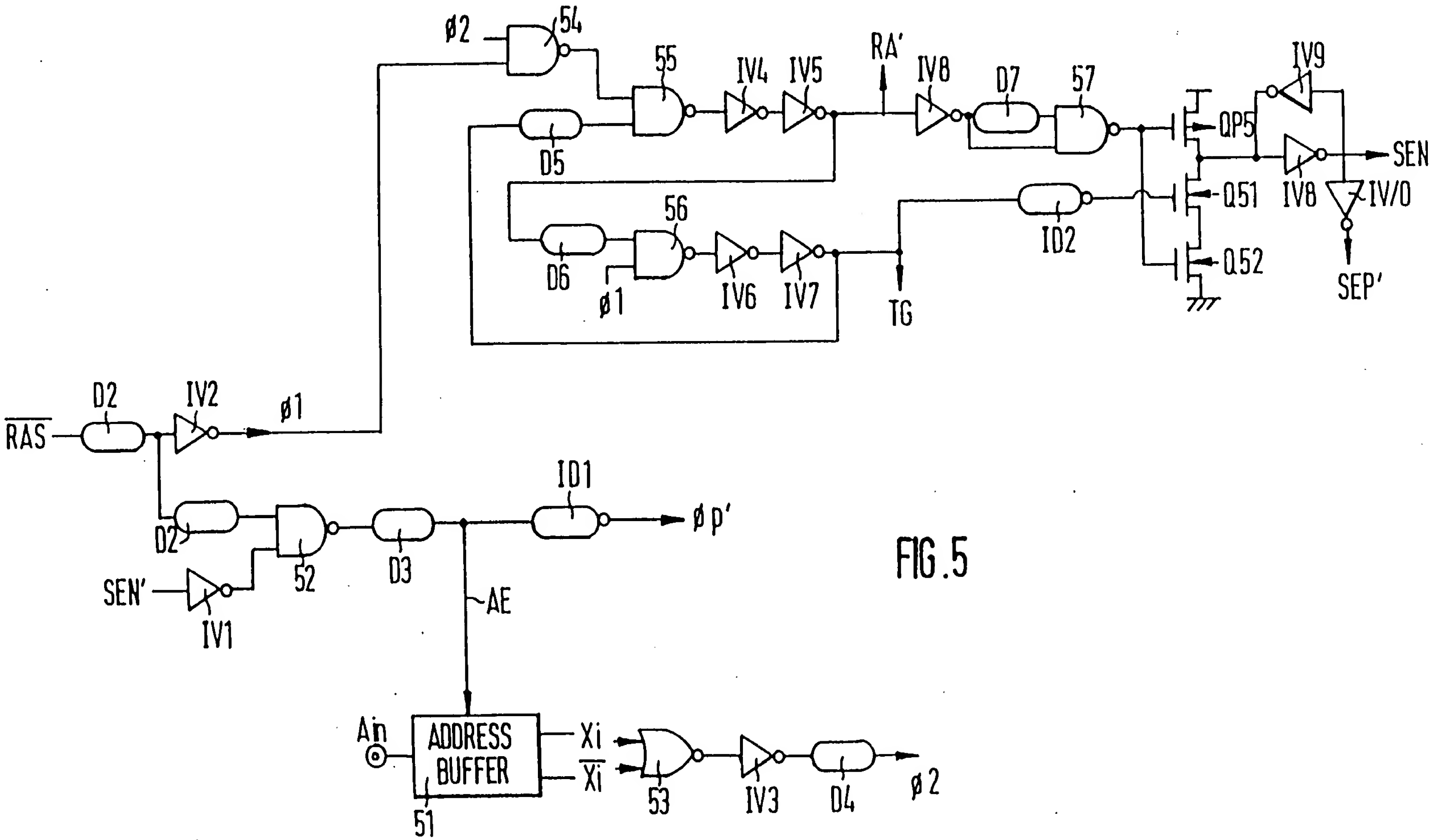

RAS
D2
IV2
ø1
ø2
54
55
IV4
IV5
RA'
IV8
D7
57
D5
D6
56
ø1
IV6
IV7
TG
ID2
QP5
Q51
Q52
IV9
SEN'
IV/0
SEP'
ID1
ø p'
D2
52
D3
SEN'
IV1
AE
Ain
ADDRESS
BUFFER
51
Xi
Xi
53
IV3
D4
ø 2

FIG.5

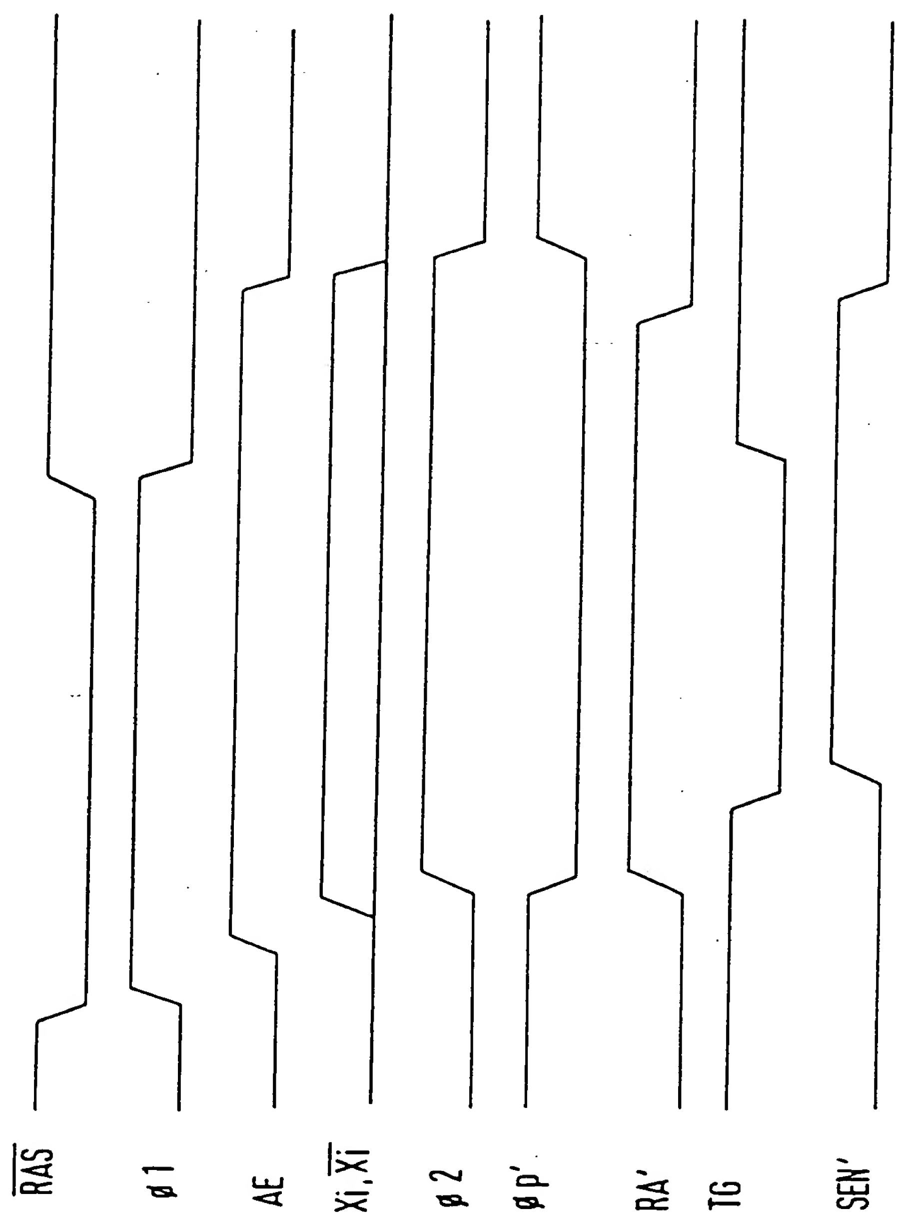
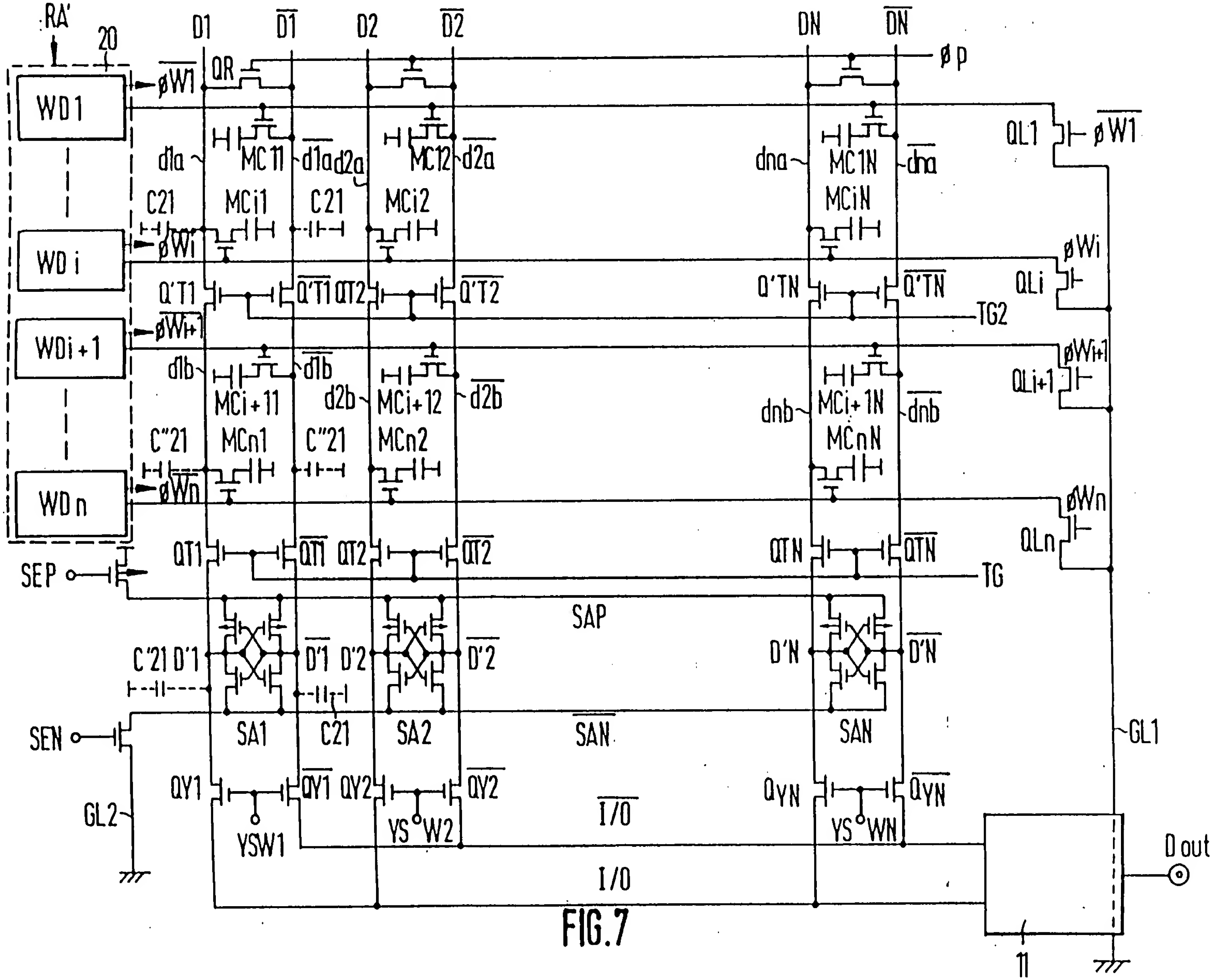


FIG.6



RA'
20
WD1
WDi
WDi+1
WDn
D1
D1
D2
D2
DN
DN
øp
QR
øW1
øWi
øWi+1
øWn
d1a
d1a
d2a
d2a
dna
dna
d1b
d1b
d2b
d2b
dnb
dnb
MC11
MC12
MC1N
MCi1
MCi2
MCiN
MCi+11
MCi+12
MCi+1N
MCn1
MCn2
MCnN
C21
C"21
Q'T1
Q'T1
Q'T2
Q'T2
Q'TN
Q'TN
TG2
QT1
QT1
QT2
QT2
QTN
QTN
TG
SEP
SAP
C'21
D'1
D'1
D'2
D'2
D'N
D'N
SEN
SA1
SA2
SAN
SAN
GL2
QY1
QY1
QY2
QY2
QYN
QYN
YSW1
YSW2
YSWN
I/O
I/O
QL1
QLi
QLi+1
QLn
GL1
Dout
11

FIG.7

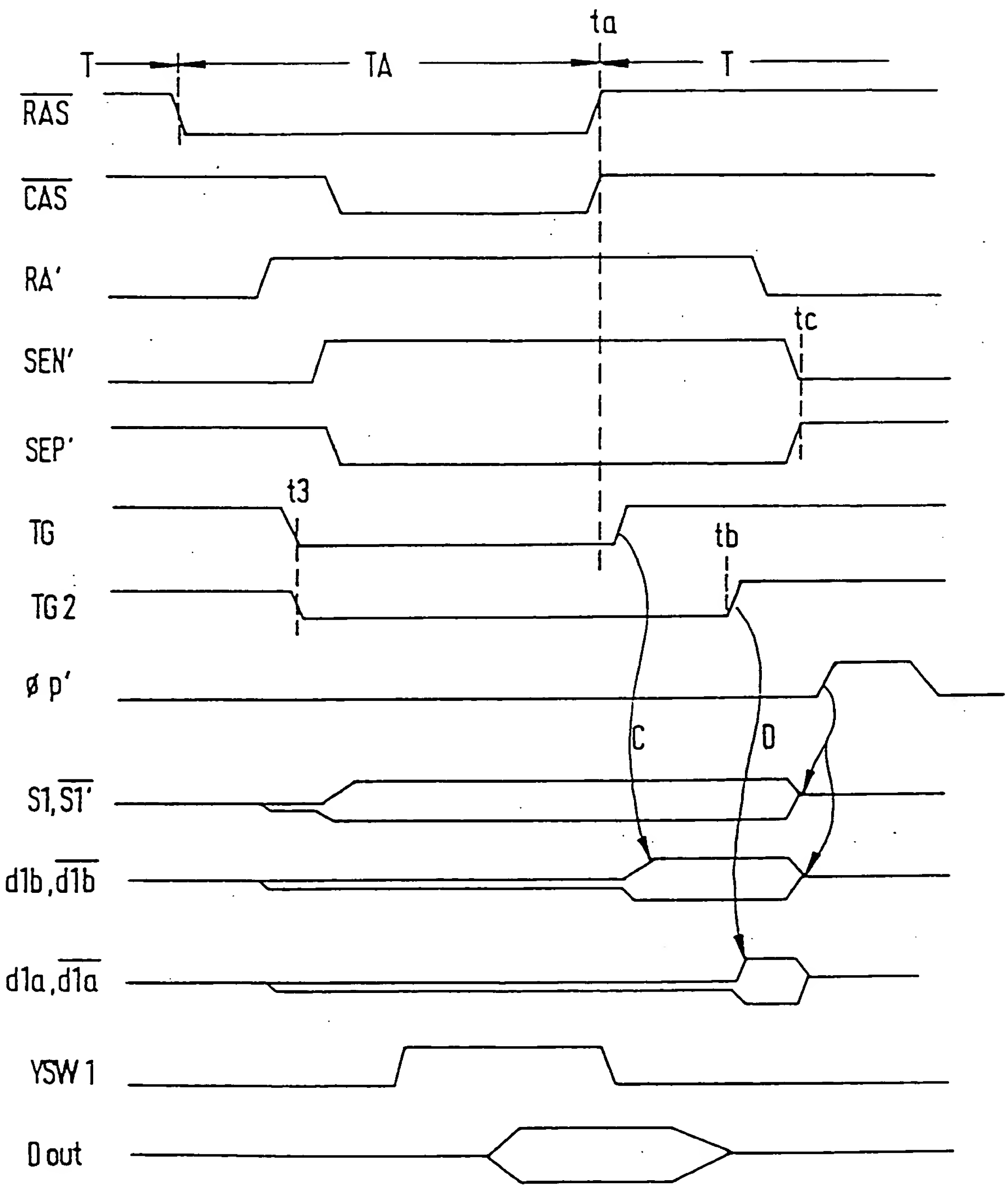

ta
T
TA
T
$\overline{RAS}$
$\overline{CAS}$
RA'
tc
SEN'
SEP'
t3
TG
tb
TG 2
ø p'
C
D
S1, $\overline{S1'}$
d1b, $\overline{d1b}$
d1a, $\overline{d1a}$
YSW 1
D out

FIG. 8

G11C11/403C1-G11C11/4..C-
G11C11/409L-

-3- = -

G11C11/409L

Office européen des brevets

(11) Publication number: **0 373 672 A3**

EUROPEAN PATENT APPLICATION

(21) Application number: 89123262.1

(22) Date of filing: 15.12.89

(51) Int. Cl.5: G11C 11/409

(30) Priority: 16.12.88 JP 317827/88

(43) Date of publication of application: 20.06.90 Bulletin 90/25

(84) Designated Contracting States: DE FR GB

(88) Date of deferred publication of the search report: 17.04.91 Bulletin 91/16

(71) Applicant: NEC CORPORATION
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

(72) Inventor: Fujii, Takeo
c/o NEC Corporation 33-1, Shiba 5-chome
Minato-ku Tokyo(JP)

(74) Representative: Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62 Liebherrstrasse 20
W-8000 München 26(DE)

(54) **Semiconductor memory circuit having an improved restoring control circuit.**

(57) A dynamic memory circuit which can operate with a reduced amount of current noise and without destruction of stored data is disclosed. The memory circuit includes dynamic memory cells necessitating restoring operation, a read circuit for performing a read-out operation in an active state and a restore circuit for performing a restore operation in a reset state following the active state.

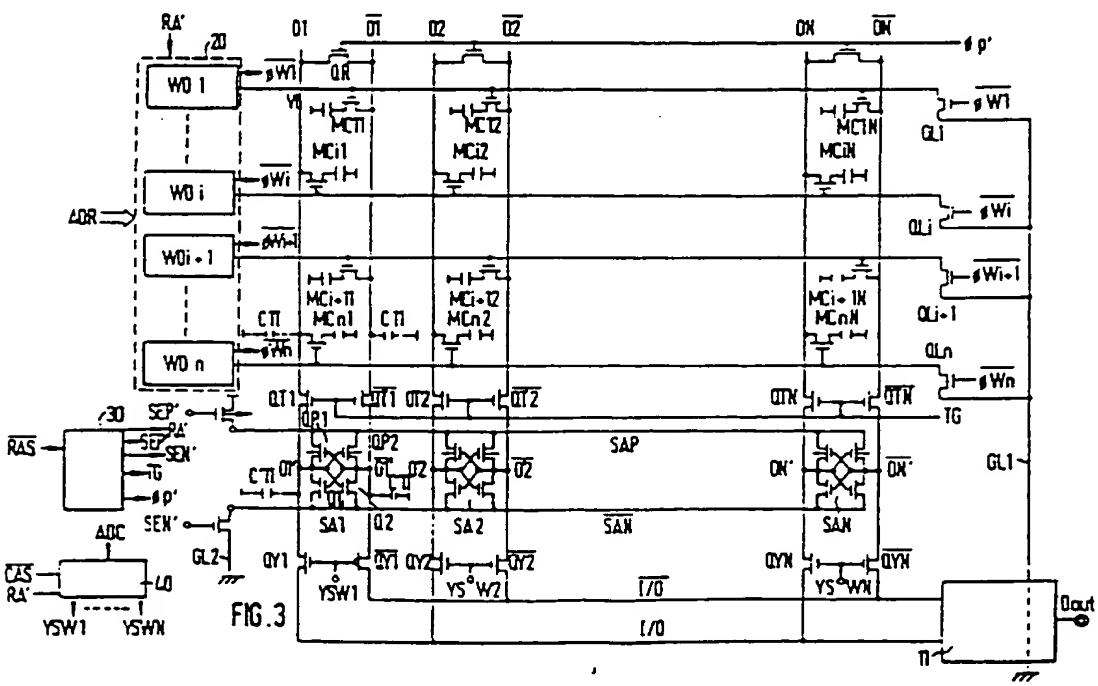


FIG.3

EP 0 373 672 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 12 3262

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 037 252 (FUJITSU) * Page 3, lines 1-25; fgure 2 *	1	G 11 C 11/409
Y	EP-A-0 240 155 (FUJITSU) * Figure 2; page 8, line 26 - page 10, line 29 *	1	
A Y	WO-A-8 607 183 (AMERICAN TELEPHONE & TELEGRAPH CO.) * Page 9, line 20 - page 10, line 27; figure 3 *	3,4 1	
A A	EP-A-0 185 572 (FUJITSU) * Page 4, line 25 - page 6, line 23; figures 2,3b *	3 4,5	
A	US-A-3 810 124 (W.K. JOFFMAN et al.) * Column 3, lines 9-47; figure 2 *	2	
P,X	EP-A-0 316 902 (NEC CORP.) * Claims 1-8 *	1,3-5	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 11 C 11

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	31 January 91	KAMSAETER K.M.S.

CATEGORY OF CITED DOCUMENTS

- X : particularly relevant if taken alone
- Y : particularly relevant if combined with another document of the same catagory
- A : technological background
- O : non-written disclosure
- P : intermediate document
- T : theory or principle underlying the invention
- E : earlier patent document, but published on, or after the filing date
- D : document cited in the application
- L : document cited for other reasons
- & : member of the same patent family, corresponding document